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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/770,478	01/29/2001	James R. Del Signore II	230 P 051	6823

7590 11/19/2002
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EXAMINER

TRA, ANH QUAN

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 11/19/2002

15

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/770,478

Applicant(s)

DEL SIGNORE II ET AL.

Examiner

Quan Tra

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4,6-8 and 17-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,6-8 and 17-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the response filed 10/28/2002. Applicant's declaration under 37 CFR 1.131 overcomes the final rejection mailed 05/31/2002. A new final rejection is introduced in view of applicant's necessitated amendment.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 6, 17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Denki (JP 10-293617) (newly cited).

As to claims 1, Denki discloses in figure 1 an inrush circuit comprising: means (Co, ZD1, S8, R3) for providing a voltage ramp; means (output node 4 and load ZL) defining an output voltage (VOUT); an operational amplifier circuit (6) having a reference input (-), the operational amplifier circuit receiving the voltage ramp at the reference input and comparing a divided sample (VR1) of the output voltage with the voltage ramp, the operational amplifier operating in a linear mode, whereby the output voltage approximate a multiple of voltage ramp; transistor means (Q1) electronically connected to the operational amplifier circuit, the transistor means operating in linear mode during capacitor charging, subsequently reaching a full-ON state; and energy storage load means (C1) connected to the transistor means for receiving a full power supply (E1) after the transistor means reaches its full-ON state.

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As to claim 2, figure 1 shows the transistor means (Q1) comprises a power FET (column 9, lines 3 teaches the powersupply is about 10-20 volts. Therefore, transistor Q1 is a power transistor).

As to claim 6, it is inherent for field effect transistor is operative initially in an OFF state, and subsequently becomes operative in a full-ON state.

As to claim 17, figure 1 shows a time delay means (X1) connected to means for providing a voltage ramp.

As to claim 19, circuit figure 1 operates about 10-20 volts which is relatively high voltage compare to CMOS voltage. Therefore, capacitor C1 must have a large capacitance in order to operate in a high voltage circuit. Therefore, capacitor C1 is a bulk capacitor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3-4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denki (JP 10-293617).

As to claim 3, figure 1 shows all limitations of the claim except for the output voltage approximates the voltage ramp by a gain of two. However, equations 4, 8 and 9 teaches $V_{out} = V_{REF}(R1+R2)/R1$ (wherein V_{REF} is the voltage ramp). It is seen as an obvious design choice for selecting $R1 = R2$. Therefore, according to the equations above the output voltage approximates the voltage ramp by a gain of two.

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As to claim 4, it is seen as an intended use for selecting the output node to be a point-of-sale printer.

As to claim 18, figure 1 shows all limitations of the claim except for the time delay means reaches threshold in 50 ms. However, it is seen as an obvious design choice for selecting the delay time of the delay means to be approximately 50 ms dependent upon particular environment of use to ensure optimum performance.

5. Claims 7 and 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Denki (JP 10-293617) (newly cited) in view of Kajimoto (USP 5557193).

Denki's figure 1 shows all limitations of the claim except for a capacitive means electronically connected to the field effect transistor for ensuring that the field effect transistor is initially operative in the OFF state. However, Kajimoto's figure 1 shows a circuit having capacitor 12 for ensuring transistor (MOUT) is initially in the OFF state and providing a good transient characteristic for the circuit. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor coupled between the output of the amplifier and output of Kinoshita's circuit for the purpose of ensuring the transistor Q1 initially in the OFF state and providing a good transient characteristic for the circuit.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

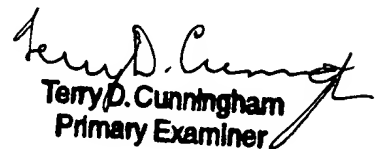
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



QT
November 12, 2002



Terry D. Cunningham
Primary Examiner